From (A9), it follows that at $kd = \pi$ ($I_p \approx 1.23$)

$$\frac{Z_a}{\tanh(\alpha_a d/2)} \approx \frac{2\pi\eta}{I_p}. \quad \text{(A11)}$$

After the substitution of (A11) into (A10), the normalized impedance of the slot is

$$Z_{sn} = \frac{2}{1.23\pi}\frac{\lambda^2}{ab}\left(\frac{\lambda_g}{\lambda}\right)^3 \cos^2\left(\frac{\pi\lambda}{4a}\right)$$

which is the classical Stevenson formula [6], [7].

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Large-Signal Equivalent-Circuit Model of a GaAs Dual-Gate MESFET Mixer

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***Abstract*—A large-signal equivalent-circuit model of a GaAs dual-gate MESFET mixer containing twelve elements, of which eight are voltage-dependent, is solved in the time domain for local oscillator and signal frequencies of 9.5 GHz and 10.0 GHz, respectively. The results give the variation of conversion gain with local oscillator and signal power levels and are in good agreement with measured values. The model is formulated in such a way that material/device/circuit interactions can be studied, yielding information on the preferred device structures and biasing conditions.**

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I. INTRODUCTION

As GaAs microwave integrated circuits emerge as viable systems, one of the most important applications is predicted [1] to be in direct broadcasting by satellite (DBS) television with worldwide market possibilities. An essential requirement for this technology is an integrated-circuit 'front-end' to be mounted on the receiving dish. The dual-gate MESFET mixer is probably the best solution to the down conversion in this system because it has the advantages of a reasonable noise figure and conversion gain (as opposed to a loss for Schottky diodes), and the inherent separation of signal and local oscillator inputs results in circuit simplification with consequent economies in chip surface area.

With this application in mind, a large-signal equivalent-circuit model of a dual-gate MESFET in a mixer configuration is presented. Using dc characteristics and analytical expressions for the voltage dependence of the capacitance of a Schottky barrier, the model is solved in the time domain over one period of the IF, and the resulting output is Fourier analyzed to determine the frequency components produced. The advantages of this method of solution are that the mixing process can be well understood and illustrated under all conditions of bias, and also the relationship between the material parameters and the circuit performance can be elucidated.

II. DERIVATION OF THE MODEL

A. Low-Frequency Model

At low frequencies, the effects of reactive components can be ignored and the mixing properties of the device derived using $I_{DS}-V_{DS}$ characteristics. In common with other published work [2], [3], the dual-gate FET is modeled here as two single-gate FET's in cascode with the dain of FET 1 connected to the source of FET 2. The signal (RF) is applied to the gate of FET 1 and the local oscillator (LO) to that of FET 2. This is illustrated schematically in Fig. 1, which also shows the important voltages used in the calculations. In order to obtain a solution to this circuit, an analytical expression for the output characteristics of each component FET is required. For this work, the expression used is based on that suggested by Gopinath and Rankin [4], i.e.,

$$I_{DS} = \left(1-\frac{V_{DS}}{V_p}\right)^2\left(I_{DSS}+\frac{V_{DS}}{R_{DO}}\right)$$

for $V_{DS} > V_{TAN}$, i.e., the saturation region (1a)

and

$$I_{DS} = \left(1-\frac{V_{GS}}{V_p}\right)^2\left[I_{DSS}+\frac{V_{DS}}{R_{DO}}-I_{DSS}\left(\frac{V_{TAN}-V_{DS}}{V_{TAN}}\right)^3\right]$$

for $V_{DS} < V_{TAN}$. (1b)

In these equations, V_p is the gate pinchoff voltage, I_{DSS} the drain–source saturation current, and R_{DO} the output resistance.

V_{TAN} defines the boundary between resistive and saturation behavior where

$$V_{TAN} = V_{OO}\left[1+\left(1+\frac{2R_{DO}I_{DSS}}{V_{OO}}\right)^{1/2}\right]$$

with

$$V_{OO} = \frac{\left(1-\frac{V_{GS}}{V_p}\right)^2 V_{DT}^2}{2(I_{DSS}R_{DO}+V_{DT})} \text{ and } V_{DT} = 2.25 \text{ V}.$$

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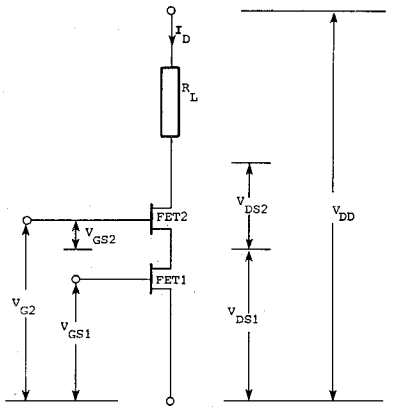

Fig. 1. Model of a dual-gate MESFET mixer showing how the device is separated into its component parts with their corresponding bias voltages.

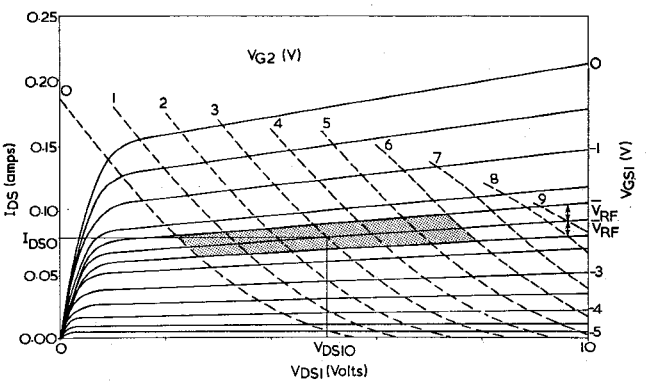

Fig. 2. Output characteristic, at $V_{DD} = 15$ V, for FET 1 with "load lines" (dashed) representing the effect of FET 2 and a load resistor of 50 Ω. The "load lines" are only shown in the region of allowed biasing. The shaded area is that swept out by the RF of amplitude V_{RF} about $V_{GS1} = 2$ V and the LO of amplitude 3 V about $V_{G2} = 3$ V.

The constants V_p, I_{DSS}, and R_{DO} can be chosen to allow for variations in device fabrication, and, indeed, they may be different for FET 1 and FET 2 in an unsymmetrical device.

The analytical $I_{DS}-V_{DS}$ expression is used for its convenience and versatility, and, providing it is a reasonable representation of the constituent FET characteristics, the essentials of the mixing process and its dependence on material parameters and bias voltages can be studied. A more accurate model would result from using characteristics derived from either measurements [5], [6] or device simulation [7].

The circuit is solved by treating FET 2 and R_L as the load for FET 1. The 'load lines' for various values of V_{G2} can be calculated and combined with the output characteristic for FET 1, as shown in Fig. 2 for $R_L = 50$ Ω. By locating the crossing points of these curves for corresponding values of V_{GS1} and V_{G2} throughout one IF cycle, it is possible to calculate I_{DS} at each time step. This process is simply and quickly implemented on a computer using (1), and the resulting time variation of I_{DS} is Fourier transformed to give the output spectrum. Although this dc model cannot give information on frequency response and conversion gain, it does have a number of useful functions. For example:

a) it gives a quick indication of the allowable limits of the bias voltages so that gates do not go too far into forward bias and source–drain voltages do not become excessive,
b) the bias conditions most likely to give a high conversion gain can be quickly located,
c) an insight into the operation of a device as a mixer including the effects of voltage swings and nonlinearities can be obtained,
d) it provides a convenient method of setting up the initial conditions for the high-frequency model, and
e) it serves as a low-frequency check on the high-frequency model.

The operating principle of the mixer can be obtained from Fig. 2. As the RF signal alters the working characteristic between $V_{GS10} \pm \overline{V}_{RF}$ (where V_{GS10} is a typical dc bias on Gate 1 and $\overline{V}_{RF}$ is the amplitude of the signal voltage), the local oscillator sweeps V_{DS1} and, hence, I_{DS} between the limits imposed by the appropriate load lines. The swept area is shaded in the figure, with $\overline{V}_{RF}$ exaggerated for clarity.

Now

$$V_{GS1} = V_{GS10} + V_{RF} \tag{2}$$

where

$V_{RF} = \overline{V}_{RF} \sin \omega_{RF} t$ and ω_{RF} is the signal frequency.

(V_{G2} is similarly defined as $V_{G2} = V_{G20} + \overline{V}_{LO} \sin \omega_{LO} t$.)

V_{DS1} will depend on both the RF and the local oscillator signals. However, because $V_{RF} \ll V_{LO}$, the direct effect of the RF signal on V_{DS1} can be ignored compared to that of the local oscillator.

Consequently

$$V_{DS1} \approx V_{DS10} + A_2 V_{LO} \tag{3}$$

where V_{DS10} is the quiescent value of V_{DS1} and

$$A_2 = \frac{\partial V_{DS1}}{\partial V_{G2}}.$$

Equation (3) is valid, provided the operation remains within the linear regions of both FET 1 and FET 2 where the load lines are approximately uniformly spaced, and therefore A_2 may be assumed to be a constant.

Applying (1a) to FET 1 and substituting for V_{GS1} and V_{DS1} from (2) and (3) gives

$$I_{DS} = I_{DSO} + \left(1 - \frac{V_{GS10}}{V_p}\right)\left[\frac{A_2 V_{LO}}{R_{DO}}\left(1 - \frac{V_{GS10}}{V_p}\right) - \frac{2 I_{DSS} V_{RF}}{V_p}\left(1 + \frac{V_{DSO}}{R_{DO} I_{DSS}}\right) - \frac{2 A_2 V_{RF} V_{LO}}{V_p R_{DO}}\right] + \text{smaller terms in } V_{RF}^2 \text{ and } V_{RF}^2 V_{LO}. \tag{4}$$

In (4), I_{DSO} is the quiescent source–drain current for the dual-gate FET and is essentially the dc component in the output. The first term in the square brackets is at the local oscillator frequency, the second at the signal frequency, and the third contains the mixing products at the sum and difference (intermediate or IF) frequencies. The smaller terms contain the image and doubling frequencies.

Selecting out the IF component, it is found that the fraction of the RF converted to the IF is given by

$$\frac{V_{IF}}{V_{RF}} \propto \frac{R_L}{(R_{DS} R_{DO})^{1/2}} \left(1 + \frac{R_{LL}}{R_{DS}}\right)^{-1} \frac{V_{LO}}{V_p} \tag{5}$$

where V_{IF} is the IF voltage developed across R_L. R_{DS} is the differential output resistance of FET 1 under the chosen bias conditions and R_{LL} is the effective resistance of the load lines in the operating region. Equation (5) has a maximum value when

$R_{DS} = R_{LL}$, given by

$$\left.\frac{V_{IF}}{V_{RF}}\right)_{\max} = \frac{R_L}{2(R_{LL}R_{DO})^{1/2}}\frac{V_{LO}}{V_p}.$$

The biasing condition required to approach this maximum (i.e., $V_{GS1} \rightarrow V_p$) results in large values of R_{LL} and R_{DO}, which in turn lowers the maximum voltage conversion available. A compromise must therefore be achieved, but improved performance is expected for lower values of R_{LL} and R_{DO} and, in particular, if FET 1 has a lower output resistance than FET 2.

The simplified analysis is only applicable at low frequencies in the linear regions, but is expected to be valid in general terms at high frequencies also. If the signal levels are such as to extend the operation into the nonlinear regions, more power is diverted into unwanted components in the output, and, in consequence, there is not necessarily a corresponding increase of the IF component.

B. High-Frequency Model

The dc model is of course deficient in the reactive circuit elements that become important at microwave frequencies—in particular, the capacitances associated with the Schottky barriers, which results in power being drawn from the RF and LO sources. Inclusion of these in the model means that a new method of solution must be used, for which we proceed as follows.

In general, for a single-gate device

$$I_{DS} = F(V_{GS}, V_{DS})$$

where $F(V_{GS}, V_{DS})$ is a function of the gate-source and drain-source voltages. Differentiating gives

$$\delta I_{DS} = \left.\frac{\partial F}{\partial V_{GS}}\right|_{V_{DS}} \times \delta V_{GS} + \left.\frac{\partial F}{\partial V_{DS}}\right|_{V_{GS}} \times \delta V_{DS}$$

which can be written

$$\delta I_{DS} = G_M(V_{GS}, V_{DS})\,\Delta V_{GS} + \Delta V_{DS}/R_{DS}(V_{GS}, V_{DS})$$

where G_M and R_{DS} are the voltage-dependent, small-signal, transconductance and source-drain resistance, respectively, and are given by

$$G_M = \left.\frac{\partial F}{\partial V_{GS}}\right)_{V_{DS}} \text{ and } R_{DS} = 1/\left.\frac{\partial F}{\partial V_{DS}}\right)_{V_{GS}}.$$

The functional forms for G_M and R_{DS} can then be found by differentiation of the $I_{DS} - V_{DS}$ expression which, for this model, gives

$$G_M = G_{MO}\left(1 - \frac{V'_{GS}}{V_p}\right) \text{ and } R_{DS} = \frac{R_{DO}}{\left(1 - \frac{V'_{GS}}{V_p}\right)^2},$$

$$G_{MO} = 48 \text{ mS and } R_{DO} = 143\ \Omega. \quad (6)$$

In (6), V'_{GS} refers to the voltage across the input capacitors C_{GS1} and C_{GS2} as appropriate.

The high-frequency model analyzed in this paper is shown in Fig. 3, with the G_M and R_{DS} of each FET given by (6), and the gate-source capacitances given by

$$C_{GS} = C_{GSO}\left(1 - \frac{V'_{GS}}{V_{bi}}\right)^{-1/2},$$

$$V_{bi} = \text{zero bias barrier height} = 0.8 \text{ V}, \quad C_{GSO} = 0.5 \text{ pH}. \quad (7)$$

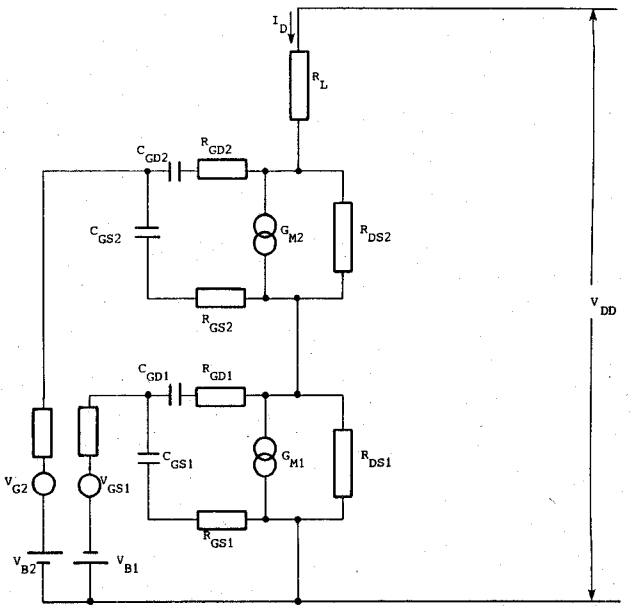

Fig. 3. Circuit used for high-frequency modeling of the dual-gate MESFET mixer.

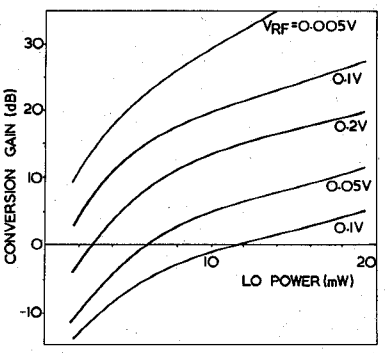

Fig. 4. Conversion gain versus local oscillator power calculated from the high-frequency model.

Also

$$R_{GS1} \times C_{GS1} = R_{GS2} \times C_{GS2} = \tau \text{ where } \tau = 10^{-12} \text{ s}. \quad (8)$$

Equations (7) and (8), with V'_{GS} replaced by V_{GD}, are also used to determine the gate-drain capacitances and resistances, which are calculated from the dc biasing conditions and held at these values throughout. The effect of the transit time of electrons under the gates can be included by a time-averaging process, but its effect is not expected to be large at the frequencies of interest and has therefore not yet been incorporated into the model.

Starting with component values calculated from the initial conditions, the program advances V_{G1} and V_{G2} in small increments. At each step, the changes in the voltages around the circuit are calculated and used to update voltage-dependent component values for the next step.

III. Results and Discussion

Solution of the model has yielded curves for the variation of conversion gain (defined as the ratio of power delivered to the load at the IF, to power supplied by the RF source) with RF power and LO power. As can be seen from Figs. 4 and 5, the conversion gain increases with the local oscillator power and decreases with the signal power. The gains achieved are also

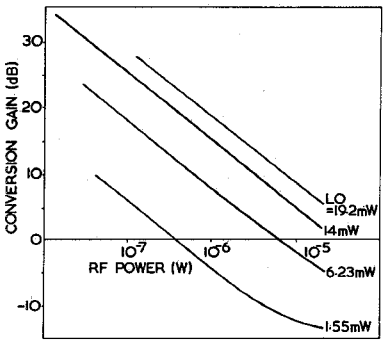

Fig. 5. Conversion gain versus RF signal power calculated from the high-frequency model.

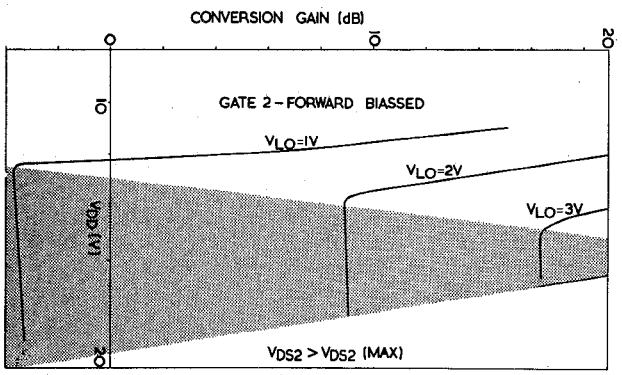

Fig. 6. Variation of conversion gain with supply voltage V_{DD} showing the region of stable operation (shaded area).

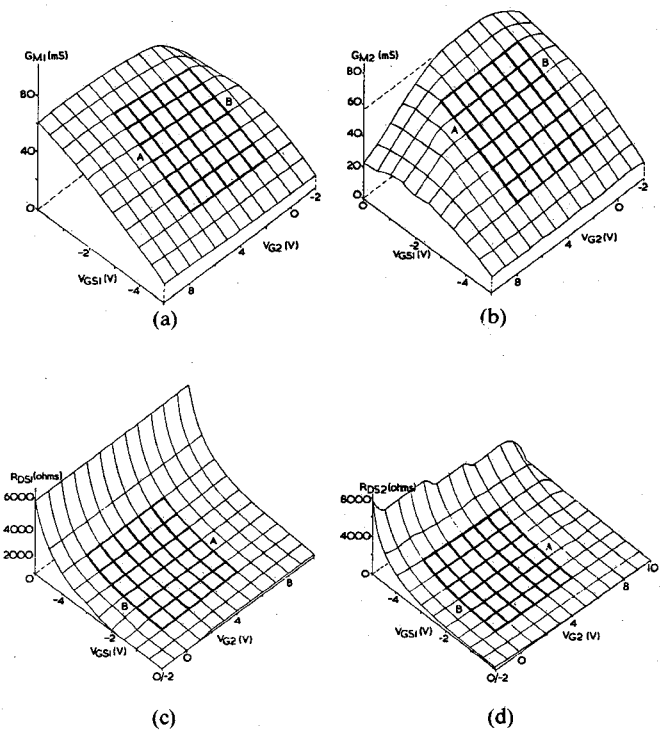

Fig. 7. Variation of (a) G_{M1}, (b) G_{M2}, (c) R_{DS1}, and (d) R_{DS2} with gate voltages V_{GS1} and V_{G2}. The accessible region is outlined in heavy lines and AB is a typical working line corresponding to Fig. 2.

consistent with measured values [8],[9], especially considering the ideal nature of the circuit analyzed and the simple resistive loading at the gates and drain.

Fig. 6 shows the effect on the conversion gain of varying the supply voltage V_{DD}. For each value of the local oscillator signal, the conversion gain first falls very rapidly and then levels out with increasing V_{DD}. Outside of these two regions, either the gate of FET 2 goes into forward bias (at low values of V_{DD}) or the source-drain voltage of FET 2 becomes too large (at high values of V_{DD}). For stable operation with respect to variations in the supply voltage, the device will best be operated in the horizontal regions of the curves as indicated by the shaded area of Fig. 6, where for the highest gains the range of permissible values of V_{DD} decreases. This figure shows that for stable, high-gain operation the bias voltages must be carefully chosen.

The results of the low-frequency modeling described by (4) show that mixing in a dual-gate FET is inherently a simple interaction between the different regions of the device resulting in a small number of frequency components in the output spectrum. This is further illustrated in Fig. 7, where it can be seen that in the operating region the device parameters are very nearly linear functions of the gate voltages. A close inspection of Fig. 7 shows that the device parameter variations are similar to those of Tsironis *et al.* [9] but cover a more limited range, approximately intermediate between their regions {1} and {2}. This mode of operation implies contributions from both component FET's to the IF, and this has been confirmed in the model. The restrictions on biasing necessary to keep both FET's in their operating regions, in this case, limits the access to the three separate operating modes as discussed in [9]. On extension of the model to high frequencies, extra components are introduced into the output owing to the nonlinear behavior of the reactive components, but the mixing process is still basically that described for the low-frequency model.

IV. Conclusions

The dual-gate MESFET mixer has been modeled to give results which, given the simplified resistive loading on the gates and drain, are consistent with measured values. Using this model, an optimum area of biasing can be designed for maximum stable conversion gain. The mixing action is shown to be the result of simple low-order processes, and its relationship to device and material parameters has been demonstrated.

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